CLAIMS

What is claimed is:

1. A memory system comprising:

a memory controller;

an interface device coupled to the memory controller via a first signal path; and

a plurality of memory elements removably coupled to the interface device via respective second signal paths, each of the second signal paths having a lower data transfer capacity than a data transfer capacity of the first signal path.

2. The memory system of claim 1 wherein the first signal path comprises a plurality of substantially parallel signal lines that extend from a first end at the memory controller to a second end at the interface device.

3. The memory system of claim 2 wherein the plurality of the signal lines is disposed within a flexible material to form a flex cable.

4. The memory system of claim 2 wherein the first signal path further comprises a plurality of shielding elements disposed adjacent individual signal lines of the plurality of signal lines to shield the individual signal lines from one another.

5. The memory system of claim 4 wherein each of the shielding elements is disposed in coaxial alignment with a respective one of the individual signal lines.

6. The memory system of claim 2 wherein the plurality of signal lines comprise conductive traces disposed on a printed circuit board.

7. The memory system of claim 1 wherein the interface device is implemented in a dedicated integrated circuit device.

8. The memory system of claim 1 wherein the data transfer capacity of the first signal path is at least as great as a sum of the data transfer capacities of the second signal paths.

9. The memory system of claim 1 wherein the first signal path comprises at least one signal line to conduct a first timing signal from the memory controller to the interface device, and wherein the interface device includes circuitry to sample signals on the first signal path in synchronism with the first timing signal.

10. The memory system of claim 9 wherein the first timing signal is a clock signal.

11. The memory system of claim 9 wherein the first timing signal is a strobe signal.

12. The memory system of claim 9 wherein the second signal paths comprise respective signal lines to conduct second timing signals from the interface device to the memory elements, and wherein the first timing signal oscillates at greater frequency than the second timing signals.

13. The memory system of claim 12 wherein the oscillating frequency of the first timing signal is an integer multiple of the oscillating frequency of the second timing signals.

14. The memory system of claim 1 wherein at least one of the memory elements comprises a memory module having a plurality of discrete memory devices mounted thereon.

15. The memory system of claim 1 wherein at least one of the memory elements comprises a plurality of memory modules coupled in parallel to the respective second signal path.

16. The memory system of claim 1 wherein at least one of the memory elements comprises a discrete semiconductor memory device.

17. A method of operation within a memory system, the method comprising:

transmitting multiplexed data from a memory controller to an interface device at a first data rate;

demultiplexing the multiplexed data into a plurality of data subsets within the interface device; and

transmitting the each of the data subsets from the interface device to a respective one of a plurality of memory elements at a second data rate.

18. The method of claim 17 wherein the second data rate is lower than the first data rate.

19. The method of claim 17 wherein the first data rate is an integer multiple of the second data rate.

20. The method of claim 17 further comprising receiving the multiplexed data within the memory controller.

21. The method of claim 17 further comprising receiving a plurality of data values from a host device, and wherein transmitting multiplexed data from the memory controller to the interface device comprises transmitting the plurality of data values to the interface device

in respective time intervals.

22. The method of claim 17 wherein demultiplexing the multiplexed data into a plurality of data subsets comprises allocating multiplexed data received in the interface device during a first time interval to a first one of the data subsets and allocating multiplexed data received during a second time interval to a second one of the data subsets.

23. An interface device for use in a memory system, the interface device comprising:
a first input/output (I/O) port to receive multiplexed data from a memory controller at a first signaling rate;
demultiplexing circuitry to demultiplex the multiplexed data into a plurality of data subsets; and
a plurality of second I/O ports to output the plurality of data subsets to respective memory elements at a second signaling rate.

24. The interface device of claim 23 wherein the second signaling rate is slower than the first signaling rate.

25. The interface device of claim 24 wherein the first signaling rate is an integer multiple of the second signaling rate.

26. The interface device of claim 23 wherein the interface device is implemented in a dedicated integrated circuit device.

27. The interface device of claim 23 wherein the demultiplexing circuitry is configured to allocate multiplexed data received during a first time interval to a first one of the data

subsets and to allocate multiplexed data received during a second time interval to another one of the data subsets.